Review and Analysis of Instrumentation Amplifier for IoT Applications

Tsz Ngai Lin, Bo Wang, and Amine Bermak
Division of ICT, College of Science and Engineering, Hamad Bin Khalifa University (HBKU), Doha, Qatar
{tngai, bwang, abermak}@hbku.edu.qa

***Abstract*—Instrumentation amplifiers (IAs) are essential circuit blocks for many precision sensor readouts. Particularlly, for IoT applications, IAs used in the sensing nodes should be of low-cost (no trimming) and energy-efficient, which is however still a challenge. As a design guidance, this paper reviewed the major IA topologies and circuit techniques proposed in the last two decades. Different trade-offs, including gain accruacy, energy consumption, noise, etc. are discussed when designing IAs for IoT applications. Meanwhile, the startup issue, which wastes a lot energy while is not considered in most IA design is raised in this paper.**

I. Introduction

Instrumentation amplifiers (IAs) are everywhere nowadays for transducers output conditioning, chemical/biomedical signal acquisition and more. For most sensors, their signal amplitudes are in the range of μV to mV together with large background interference such as common-mode signal and noise. IAs are specifically designed to fulfill the needs of amplifying small differential signals while rejecting noise and large interferences [1]. To meet the application requirements, IAs should exhibit finite, accurate and stable gain, μV or even nV offset, high common-mode rejection ratio (CMRR), high input impedance and low noise [2]. For future sensor nodes, multiple sensors will be integrated on the same substrate or in the same package. Such sensor node may only be powered by solid-state batteries or energy harvesters, which strictly limits the energy consumption of the interface IAs [3].

With the advance of CMOS fabrication technology, designs with >100 dB CMRR, tens of nV/$\sqrt{}$Hz noise density and μW power consumption are reported [3], [4]. Despite the improvement of IAs, which can be observed from the trend of noise efficiency factor (NEF), physical limits are almost reached. Theoretically, the minimum NEF is about 2.02 if the input transistors of the operational transconductance amplifier (OTA) in the IA are biased in sub-threshold regions [5]. However, IAs with smaller NEF does not necessary imply lower energy consumption in IoT nodes. Since most IoT sensors work discontinuously, the energy consumption of IA settling or starting-up before signal readout should be taken into account as well [6]. The slow startup process may burn more energy than the standard readout but it is not reflected in the NEF. Besides, the gain of IAs should be stable and precise because obtaining better gain accuracy through intensive device trimming would heavily increase the cost of the sensor node [1], which is not accounted in the NEF either. All the situations mentioned above mandate designers to carefully examine before selecting any IA topology for IoT applications, which motivates the review and discussion in this paper.

In this paper, a comprehensive review and summary of IA topologies is presented. Performance metrics of IA are discussed while concerns in IA settling and gain precision are raised to assist designers to choose the suitable IA topology for specific applications. This paper is organized as follows; section II summarizes the four main IA topologies. Section III analyses different parameters, focusing on the relationship and tradeoff between them. Section IV concludes the paper.

II. Different IA Topologies

Since the concept of IA came out, different topologies were proposed to achieve better performance in amplifying signals to compatible levels while rejecting unwanted common-mode signals. Four topologies will be examined in the following section, including the original switched-capacitor IA [7], the 3-opamp IA using voltage feedback, which becomes the common approach in industry [8], and the recently reported current-feedback IA [9] and capacitively-coupled IA [4].

A. Switched-Capacitor IA

The topology of a switched-capacitor IA is shown in Fig. 1(a). Two phases are required to complete one single operation. In phase ϕ_1, the input voltage will be stored in the sampling capacitors $C_{\text{in1,2}}$, while the offset of the amplifier A_1 will be stored in the offset cancellation capacitors $C_{\text{oc1,2}}$. In phase ϕ_2, a charge distribution occurs between the sampling capacitors $C_{\text{in1,2}}$ and the feedback capacitors $C_{\text{fb1,2}}$. Since the sampling plates of $C_{\text{in1,2}}$ are shorted together, the input common-mode component is effectively cancelled and, CMRR up to 120 dB can be achieved with rail-to-rail input common-mode [7].

However, the switched-capacitor structure limits the amplifier performance. Since the amplifier gain is defined by $C_{\text{in}}/C_{\text{fb}}$, the gain precision is limited by the capacitor mismatch. Large sampling capacitor is required to maintain the IA noise in nV/$\sqrt{}$Hz-level, which leads to low input impedance. Also, the charge injection and clock feed-through of the switches induce sampling noise (kT/C) [10], which degrades the amplifier precision.

B. Amplifiers with Voltage Feedback

The 3-opamp IA topology uses resistors to form a voltage feedback and achieves a constant gain. Fig. 1(b) shows the block diagram of a classical 3-opamp IA. The first stage

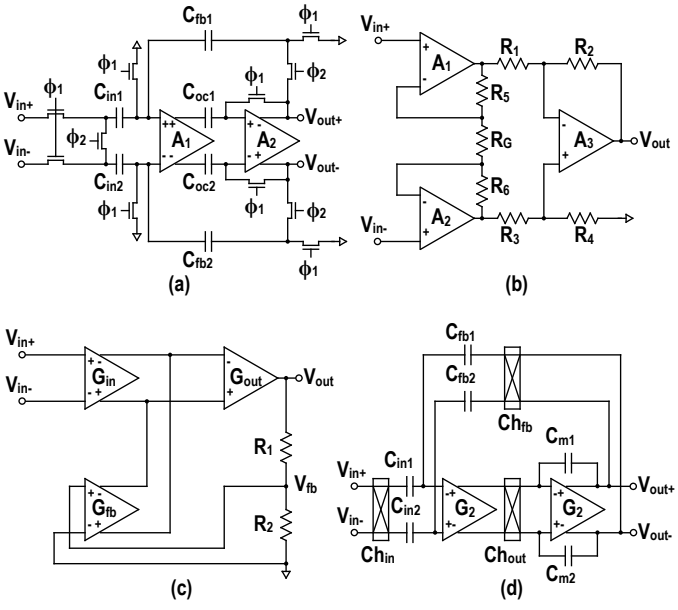

Fig. 1: Reviewed IA Topologies: (a) Switched-capacitor IA; (b) Three-Amp IA; (c) Current-feedback IA; (d) Capacitively-coupled IA.

used two opamp A_1 and A_2 to buffer the input voltage. One differential amplifier is used in the second stage to amplify the differential voltage while rejecting the common-mode voltage. Using (1), only one gain resistor $R_{\rm G}$ is required to set the amplifier gain if $R_{1\text{-}6}$ are matched.

$$V_{\rm out} = \frac{R_2}{R_1}\left(1 + \frac{2R_5}{R_{\rm G}}\right)\left(V_{\rm in+} - V_{\rm in\text{-}}\right) \tag{1}$$

Since the inputs are buffered, this topology provides good linearity and high input impedance [8]. However, A_1 and A_2 clip the input common-mode range as they cannot handle signals beyond the supply rail [4]. Moreover, in order to achieve >80 dB CMRR, laser-trimmed thin-film resistors are required for matching $R_{1\text{-}6}$ which increase the cost [10]. Furthermore, 3-opamp IA is not very power efficient as two low-noise high-gain opamps are required in the first stage.

C. Amplifiers with Current Feedback

Current-feedback instrumentation amplifier (CFIA) is the most frequently used topology for precision IAs because it provides high CMRR and high input impedance while maintaining a wide-common-mode input range. A typical CFIA consists of input and output transconductors $G_{\rm in}$ and $G_{\rm out}$ incorporated with a feedback $G_{\rm fb}$. As shown in Fig. 1(c), the input voltage $V_{\rm in}$ and the feedback voltage $V_{\rm fb}$ are converted to current via $G_{\rm in}$ and $G_{\rm fb}$ respectively. The large $G_{\rm out}$ and the feedback loop guarantee $V_{\rm in}G_{\rm in}$=$V_{\rm fb}G_{\rm fb}$. By matching $G_{\rm in}$ and $G_{\rm fb}$ in (2), the gain can be set by $R_{1,2}$ [11].

$$V_{\rm out} = \frac{G_{\rm in}}{G_{\rm fb}}\left(\frac{R_1 + R_2}{R_2}\right)\left(V_{\rm in+} - V_{\rm in\text{-}}\right) \tag{2}$$

CFIA uses both isolation and balancing techniques to achieve high CMRR [1]. Since $G_{\rm in}$ provides high output impedance, input common-mode voltage only induces a small common-mode current and can be easily cancelled out at the feedback node. CMRR above 120 dB can be obtained as the indirect current feedback isolates the input and output common-mode voltage [12].

The gain accuracy of CFIA is determined by the matching between the input and feedback transconductors $G_{\rm in}$ and $G_{\rm fb}$. CFIA can normally achieve a gain precision of 0.1% [1]. However, a total of three transconductors is needed, the high-power consumption of CFIA limited its usage in low power design.

D. Amplifers with Capacitively-Coupled Chopper

The topology of capacitively-coupled IA with chopper-stabilization was recently reported, especially for bio-potential sensing [4]. As shown in Fig. 1(d), capacitively-coupled chopper instrumentation amplifier (CCIA) consists of an operational amplifier with a capacitive feedback network. Similar to switched-capacitor IA, the gain of CCIA is set by $C_{\rm in}/C_{\rm fb}$.

By implementing an input chopper $Ch_{\rm in}$ before amplification and an output chopper $Ch_{\rm out}$ after amplification, the input signal is first shifted to high frequencies then amplified and shifted back, while the amplifier offset and 1/f noise only shifted to high frequency. After filtering, the offset and 1/f noise from amplifier can be removed.

CCIAs are more suitable for low power design as there is no transconductors in the feedback loop. The complementary switches in the input stage also give CCIA the capability of rail-to-rail sensing. However, the nonlinearity of capacitors will degrade the CMRR at a higher level of input differential voltage [10]. The input impedance of the CCIA is limited by the input capacitor and chopping frequency to MΩ-level. Positive feedback loop can be added to boost the input impedance by cancelling the current draw from the signal source [4]. However, precise capacitor in the feedback loop can only be obtained by trimming or external tuning.

III. Metrics Analysis

The performances of latest IA designs are summarized in Table I. For IoT application, low cost, low power, low noise and fast start-up settling are desired. Different metrics are examined in the following, along with some existing techniques to enhance such metric.

A. CMRR

The classical 3-opamp with careful layout design and extra trimming can only achieve 80 dB CMRR [11]. Attentions are paid to CFIA and CCIA recently because for precise signal acquisition, IAs should have >120 dB CMRR [1], [6]. Among all the topologies, CFIA is excelling in CMRR because of the isolation and high impedance of the input transconductor. To further improve CMRR, several techniques can be applied to IA. Using laser-trimmed thin-film resistors can improve CMRR through better gain matching but at the expense of higher cost. A combination of chopping and offset cancellation techniques can also be used to achieve >130 dB CMRR [12].

TABLE I: PERFORMANCE SUMMARY AND COMPARISON OF THE STATE-OF-THE-ART IAS

Design	2017 TCASI	2015 ICCSS	2012 JSSC	2012 TCASI	2012 AD8237	2011 JSSC	2011 JSSC	2009 JSSC
Technology	0.32µm CMOS	0.35µm CMOS	0.7µm CMOS	0.18µm CMOS	CMOS	0.7µm CMOS	65nm CMOS	0.7µm CMOS
Type	CFIA	CCIA	CFIA	CFIA	CFIA	CFIA	CCIA	CFIA
VDD (V)	3.3	3	5	1.8	1.8	5	1	5
Power (µW)	561	40.5	715	207	207	1450	1.8	1150
Input referred noise (nV/√Hz)	18	26	21	70	68	17	60	15
CMRR (dB)	120	110	137	130	106	127	134	120
NEF	10.6	3.7	9.6	29	28.1	11.2	3.3	8.8
PEF	270.4	40.7	469.1	1508.9	1424	623.4	9.6	384.9
Area (mm^2)	0.57	0.061	1.8	2.5	-	5	0.1	-

B. Input Bias Current

The input bias current of CMOS transistors is at pA-level but highly depends on temperature and adopted technology. When choppers are included, the input bias current increases significantly due to the charge injection and clock feed-through. Taken the high input source impedance into account, 1 nA input bias current can produce 100 μV offset voltage, which is already larger than the IA's own offset [2].

In order to maintain an acceptable input bias current ($<$100 pA), designers need to be aware that the current source should be biased in strong inversion and the chopping frequency should never exceed few hundreds kHz [2]. An on-chip charge mismatch compensation circuit is also suggested in [13] to further reduce the input bias current by using additional coupling capacitors and switch driving inverters.

C. Input Offset

Chopping is the standard approach to reduce the IA offset. Compared with auto-zeroing, which suffers from aliasing and noise folding during sampling, chopping shifts the input offset and low-frequency noise to the chopping frequency (tens to hundreds kHz) while maintaining the broadband noise characteristics, suppressing the flicker noise and voltage drift.

However, the ripple occurs at the output after chopping is a concern and techniques such as double sampling, notch filtering, ripple reduction loop, auto-correction feedback loop or trimming are required to suppress this ripple [2]. AC-coupled ripple reduction loop is suggested in some literature to sense and feedback the modulated ripple at the output to cancel the initial offset through a local feedback loop [4], [14].

D. Gain Accuracy

Gain accuracy indicates how close the measured gain is to the pre-set value. For precision IAs, gain accuracy of 0.1% is typically required and the gain should be insensitive to PVT variation [1]. For different topologies, the amplifier gain is defined differently, either through resistance or capacitance ratios.

The gain of both switched-capacitor IA and CCIA are defined by the ratio of the input capacitance and the feedback capacitance. With the development of lithography technology, the capacitance matching is mainly determined by the process spread and variation. Thus, the gain accuracy of standard switched-capacitor IA and CCIA can be expected to be about 0.1% with no trimming, which is acceptable for precision IA applications [4].

The 3-opamp IA approach implemented a voltage feedback network and the gain is set by a single resistor. Industry used laser trimmed on-chip thin film resistor to reduce the gain error to 0.3%. However, the gain drift with temperature is still significant (tens of ppm/°C) and the metal film resistors usually exhibit 1% resistance variation [15].

On the other hand, the gain accuracy of CFIA is limited by the mismatch of the input and feedback transconductor. To improve the gain accuracy, low threshold cascode transistors can be used in the input stage to minimize the gain error but not better than 0.5% matching. Another way is to apply source degeneration on the input pair with resistors, then the input transconductance is set by resistors with an untrimmed precision of 0.1% [11]. To further increase the gain accuracy, a dynamic element matching (DEM) technique is proposed at the expense of extra ripple reduction circuits in [1].

E. Noise

The noise efficiency factor (NEF) was introduced to compare the performance of different IA designs. It is defined by comparing the input-referred noise $V_{\text{rms,in}}$ of the IA with the thermal noise of a bipolar transistor or MOSFET.

$$NEF = V_{\text{rms,in}}\sqrt{\frac{2 \cdot I_{\text{total}}}{\pi \cdot U_{\text{T}} \cdot 4kT \cdot BW}} = \tilde{V}\sqrt{\frac{2 \cdot I_{\text{total}}}{\pi \cdot U_{\text{T}} \cdot 4kT}} \quad (3)$$

where I_{total} is the IA supply current, U_{T} is the thermal voltage, and BW is the bandwidth of the IA.

NEF can also be expressed by replacing $V_{\text{rms,in}}$ with its noise spectrum $\tilde{V}$ in V/$\sqrt{}$Hz to cancel the bandwidth term. Considering the different supply voltages in different designs, a modified metric, power efficiency factor (PEF) was proposed using $\text{NEF}^2 \cdot \text{VDD}$ [16].

Several IA topologies are proposed to obtain a better noise performance. Inverter-based OTA enables design with ultra-low supply voltage and the simple two-transistor structure reduces the total input noise [3]. By doubling the input transistor transconductance, current-reuse methodology reduces the NEF by $\times$1.4. Other techniques like stacked transistors and partial OTA-sharing also improved the NEF [17].

The bandwidth of IA used in sensor node is usually small ($<$1kHz). The dotted line in Fig. 2 shows the relationship between NEF and GBW. IAs with lower gain-bandwidth give smaller NEF in general. However, IA with lower NEF does not mean that it consumes less energy especially for IoT application, as explained below.

F. Settling Time

Settling time of existing IAs (μs-level) is by far incomparable to standard opamps (ns-level) [6]. Due to the large ripples generated at chopping frequency and the charge injection in

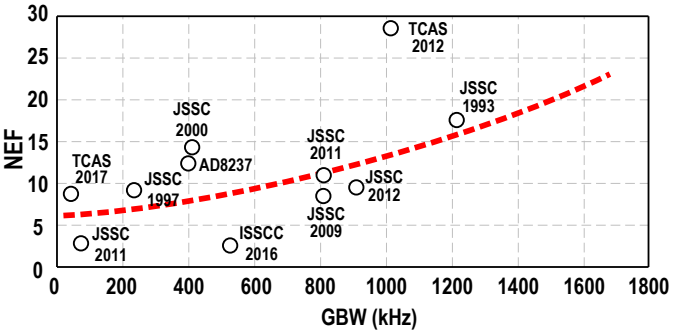

Fig. 2: NEF vs. GBW for state-of-the-arts IAs.

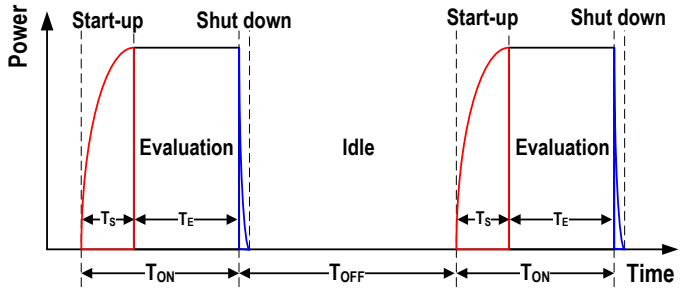

Fig. 3: Illustration of the discontinuous operation and start-up process of a low-power device in the IoT node.

switching, the system stability is a big concern and requires long duration for settling. As a result, the actual bandwidth of IAs is much lower than standard amplifiers. Particularly during start-up, amplifiers always present a slow-settling ripple at the chopping frequency. For IoT applications, however, IAs operates discontinuously and the active time is short. As shown in Fig. 3, the settling time T_S should be minimized to reduce the energy wasted during start-up process.

In order to minimize the settling time, a multi-path architecture is proposed in [2]. Since the ripple reduction loop introduces notch in the low-frequency path, a frequency compensation network helps merging the two different frequency paths to blur the notch and turns the system into first-order. As a result, the overall IA bandwidth is greatly increased. With a 100-mV input step, the proposed CFIA has a settling time of 2.5 μs with 100 pF load. However, the hidden risk of pole-zero doublets from layout mismatch may still lengthen the settling.

Similar techniques were applied to a chopped amplifier to achieve fast settling (4 μs to 0.01%) with larger signal input (4 V step) [6]. A window comparator is used to detect any opamp non-linear operation such as saturation or slewing. By keeping the opamp in linear operation, the slow low-frequency path will not affect the large-signal settling. However, if the current dissipation (1.65 mA) is scaled into μA-level, the settling time will exceed ms-level. Based on the existing IA designs which presents good noise, gain and offset performance, further research on reducing their start-up time is necessary for future IoT applications, which are mostly battery-powered.

IV. Conclusion

This paper presents a comparative review and analysis between IA topologies with their structural difference and featured performance. Standard metrics of IAs including gain, offset, noise and CMRR are discussed individually, together with some circuit techniques proposed in the literature. Besides topologies, priority of standard figures of merit (FoM) like NEF and CMRR needs to be reconsidered along with non-trimming gain accuracy and settling time to achieve low cost and high energy efficiency for IoT applications.

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